Smart camera design for realtime High Dynamic Range imaging

P.J. Lapray, B. Heyrman, M. Rossé & D. Ginhac

LE2I UMR 5158, Univ Burgundy, Dijon, France
Email: Pierre-Jean.Lapray@u-bourgogne.fr

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Summary

What is HDR imaging ?

- High Dynamic Range
- Dynamic Range is measured in Exposure Value (EV) differences or stops between the brightest and the darkest parts of the image. An increase of one stop is doubling the amount of light of the image

Capture limitation

A standard camera is able to capture only a fraction of the visual information.

What is HDR imaging ?

- For a digital camera, number of stops = bit precision of the ADC (ex : 10 stops for a 10-bit camera) camera
- Real scenes includes sunlit and shaded areas. When capturing a scene, the camera is unable to store the full dynamic range of the scene.

VS

What is HDR imaging ?

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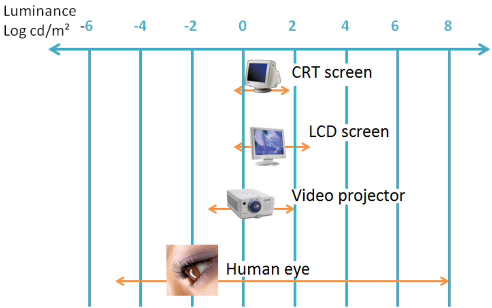
Limitation on display

- Human eyes perceives a greater Dynamic Range than a digital camera (12 orders of magnitude)
- The standard screens can not transmit to the human eye this dynamic range.



What is HDR imaging ?

- At left, an HDR image consisting of details in dark and illuminated areas
- Below, the acquisitions made by a camera.

What is HDR imaging ?

Final goal

By limiting the exposure time, the resulting image contains the details in high illumination areas. By increasing the exposure time, the resulting image contains the details in the dark areas.

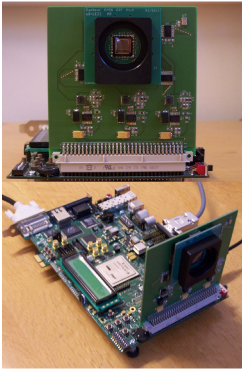
figures/hdr2.jpg

What's our goal ?

- Build a dedicated hardware camera on FPGA
- Perform multiple captures, HDR blending, tone mapping and displaying HDR contents
- 60 images/s image processing in real-time
- 1.3 Megapixels

Our hardware platform

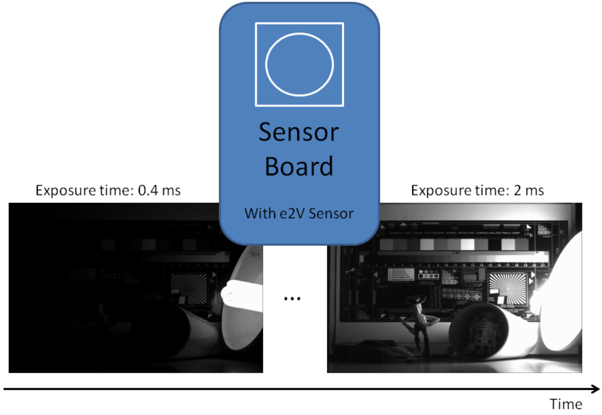
- A Virtex 5 FPGA development board
- e2V sensor : 1.3 Megapixel, 60 images/s, high sensitivity, low power, global shutter mode
- Several communication interfaces : Ethernet, SDRAM (256MB), serial interface, DVI...



Summary

HDR capture

- The sensor is able to send successively 2 images with 2 different integration times at 60 frames/s
- The integration time varies rapidly during the capture



Memory Management

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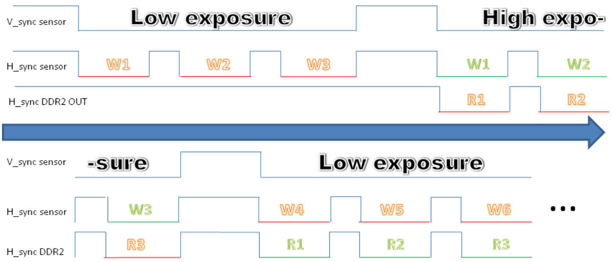
Frame buffering for HDR creating

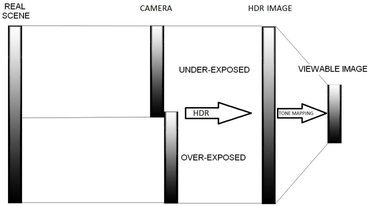
- While we receive one frame from the sensor, we read the last frame from the SDRAM memory and we write the current frame into DDR2 memory
- Finally, we have a 2 streams of Low Dynamic Range images in parallel



HDR Blending

Steps of Debevec et al. algorithm

- Having two images : one underexposed and one overexposed
- Knowing the two exposure times
- Knowing the response curve of the sensor
- Applyiing Debevec algorithm for each pixel
- We obtain an HDR image encoded with IEEE754 floating point standard



HDR Blending

Debevec et al. algorithm

$$\ln E_i = \frac{\sum_{j=1}^{P} \omega(Z_{ij})(g(Z_{ij}) - \ln \Delta t_{ij})}{\sum_{j=1}^{P} \omega(Z_{ij})} \quad (1)$$

Where $\omega(z)$ is the weighting function. It is a simple hat equation. E_i is the irradiance, Z_{ij} is the pixel value of pixel location number i in image j and Δt_{ij} is the exposure duration. The function g is defined as $g = \ln f^{-}1$. The response curve g is determined by resolving a complex quadratic function in C++.

HDR Blending

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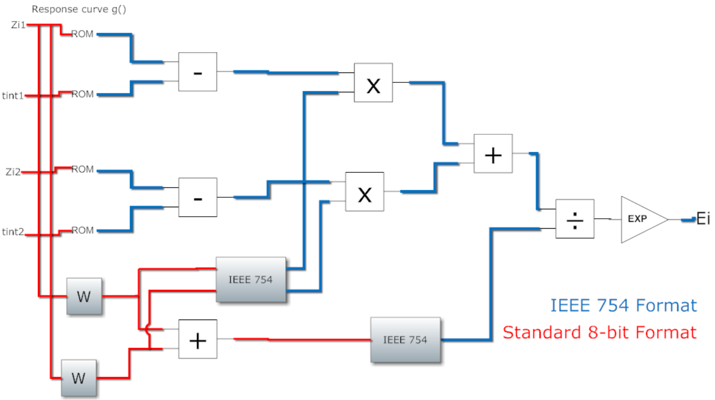

HDR Blending

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Debevec et al. algorithm

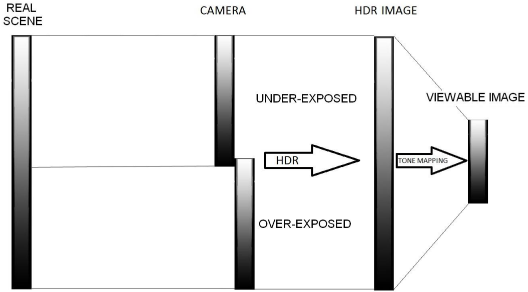
Device :	xc5vfx70t-1ff1136
Number of Slice LUTs :	5647/44800 (12%)
Number of Slice Registers :	5975/44800 (13%)
Number of Block RAM/FIFO :	6/148 (4%)
Number of DSP48Es :	4/128 (3%)
Maximum frequency :	184.536 MHz

TABLE : Summary of hardware synthesis report

Tone mapping

Make the picture viewable : the tone mapping

- Skip IEEE754 32-bit format to 8-bit
- Allow on-screen standard display
- It is necessary to convert the HDR values to 8-bit integer values in such a way that all the details are still faithfully reproduced : we use the Duan et al. global algorithm.

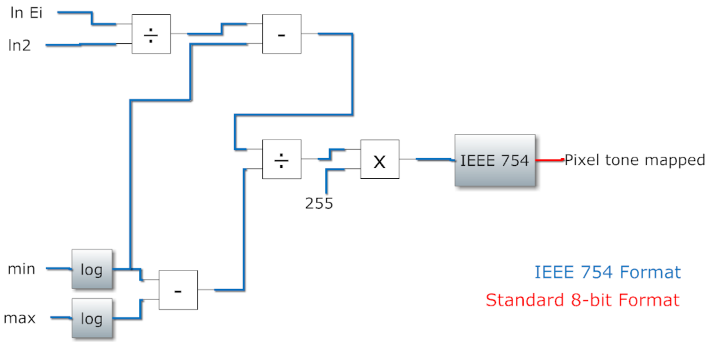


Tone mapping

Duan et al. algorithm

$$D(I) = C * (D_{max} - D_{min}) + D_{min}$$
$$with\ C = \frac{\log(I + \tau) - \log(I_{min} + \tau)}{\log(I_{max} + \tau) - \log(I_{min} + \tau)} \quad (2)$$

Duan et al. algorithm



Tone mapping

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Duan et al. algorithm

Device :	xc5vfx70t-1ff1136
Number of Slice LUTs :	4784/44800 (11%)
Number of Slice Registers :	5025/44800 (10%)
Number of DSP48Es :	2/128 (1%)
Maximum frequency :	161.125 MHz

TABLE : Summary of hardware synthesis report

Results

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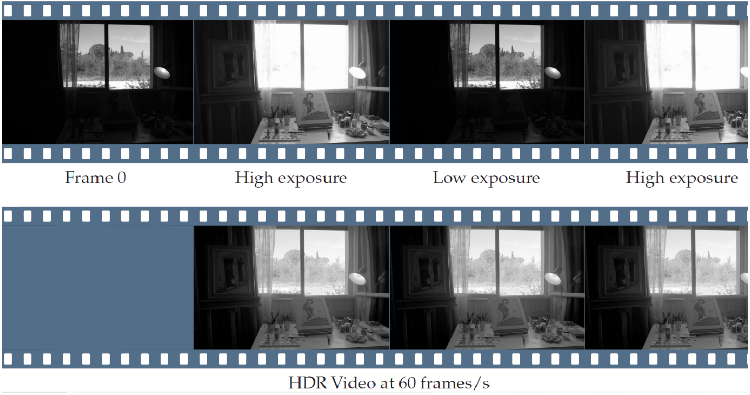

Summary

Demo

- 2 frames
- Real-time architecture
- Ability to provide data treated or partially treated from scene (Dynamics of the scene, optimum exposure times, HDR, HDR video, streaming video ...)

Future

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- We work on HDR creating from 3 images for better results
- An UDP Ethernet communication
- Implementation of more complex tone mapping algorithm.

Thank you

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Thank you.